

24-Bit Analog-to-Digital Converter (ADC) for Weigh Scales

DESCRIPTION

HX710 is a 24-bit A / D converter chip specially designed for high-precision electronic scales. Compared with other chips of the same type, this chip has the advantages of high integration, fast response speed and strong anti-interference. The overall cost of the electronic scale is reduced, and the performance and reliability of the entire scale is improved.

The gain of the input low-noise amplifier is 128.

When the reference voltage VREF is 5V, the corresponding full-scale differential input signal amplitude is 20mV. The on-chip clock oscillator does not need to be

Any external devices. The digital temperature sensor of HX710A can directly read the temperature in the chip, that is, the temperature in the system. HX710B can be used to detect the battery voltage by detecting the voltage difference (DVDD-AVDD).

All control signals are driven by pins without programming the registers inside the chip. The MCU only needs 2 I / O ports to achieve all the control of the ADC, including power-off control. The power-on auto-reset function simplifies the initialization process at startup.

FEATURES

- On-chip direct temperature measurement and digital output (HX710A)
- (DVDD-AVDD) voltage difference measurement (HX710B)
- On-chip low noise amplifier with gain of 128
- On-chip clock oscillator does not require any external components
- Power-on automatic reset circuit
- Simple digital control and serial communication: all controls are managed by pin input, no programming of on-chip registers required
- Optional 10Hz and 40Hz output data rates
- Simultaneous suppression of 50Hz and 60Hz power interference
- Power consumption:
 - Typical operating current: 1.2mA,
 - power-down current: < 1 μ A
- Operating voltage range: 2.6 ~ 5.5V
- Operating temperature range: -40 ~ + 85 $\text{ }^{\circ}\text{C}$
- 8-pin SOP-8 or DIP-8 package

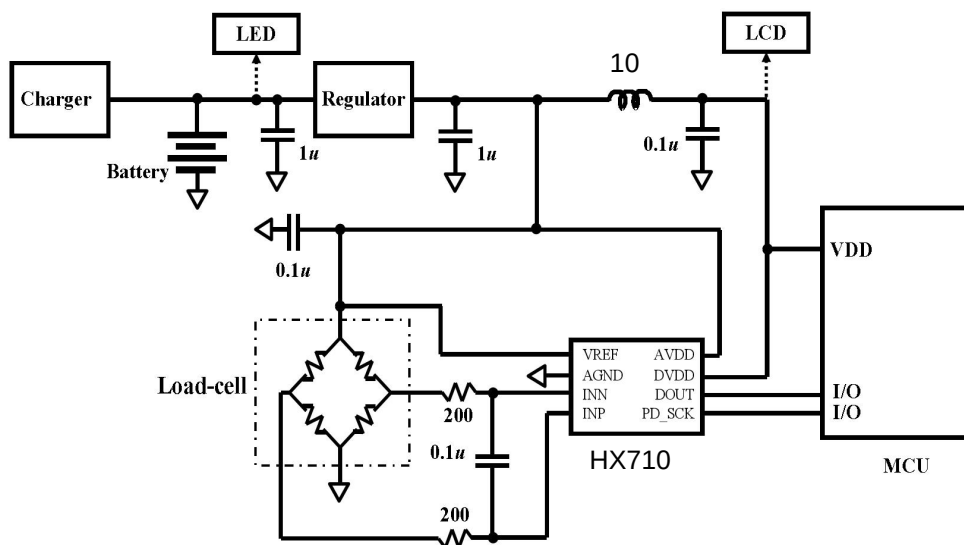
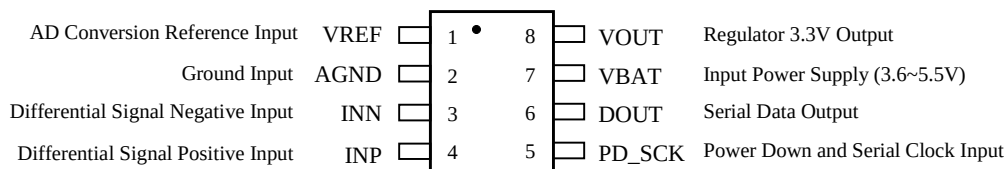


Fig. 1 Typical weigh scale application using HX710

Pin Description



SOP-8 Package

Pin #	Name	Function	Description
1	VREF	Analog Input	A / D conversion reference voltage input (1.8V -AVDD)
2	AGND	Ground	Analog Ground
3	INN	Analog Input	Differential signal negative input
4	INP	Analog Input	Differential signal positive input
5	PD_SCK	Digital Input	Power down control (high active) and serial clock input
6	DOUT	Digital Output	Serial data output
7	DVDD	Power Input	Regulator input power supply: 2.6 ~ 5.5V
8	AVDD	Power Output	Regulator output power supply: (2.6 ~ 5.5V), AVDD voltage should not be higher than DVDD voltage

Table 1 Pin Description

KEY ELECTRICAL CHARACTERISTICS

Parameter	Notes	MIN	TYP	MAX	UNIT
Full scale differential input voltage range	V(inp)-V(inn)	±0.0039*VREF			mV
Effective-Number-of-Bits (ENBs) ⁽¹⁾	Gain=128, Rate=10SPS	19.5			Bits
	Gain=128, Rate=40SPS	18.4			
Noise-Free Bits (NFBs) ⁽²⁾	Gain=128, Rate=10SPS	17.1			
	Gain=128, Rate=40SPS	16.0			
Integral Nonlinearity (INL)	Differential input, end-point fit	±0.001			%of FSR
Common mode input range		AGND+0.9		AVDD-1.3	V
VREF input voltage range		1.8		AVDD	
Output data rate		10/40			Hz
Output data coding	2's complement	800000		7FFFFFFF	HEX
Output settling time ⁽³⁾		400/100			ms
Input offset		0.01			mV
Input referred noise		50			nV(rms)
Temperature drift	Input offset	±15			nV/°C
	Gain	±7			ppm/°C
Input common mode rejection		100			dB
Power supply rejection		100			dB
Power supply voltage	DVDD	2.6		5.5	V
	AVDD	2.6		5.5	V
Analog supply current	Normal	1100			μA
	Power down	0.3			
Digital supply current	Normal	100			μA
	Power down	0.2			

(1) (2) ENBs = $\ln(FSR/RMS\ Noise)/\ln(2)$, NFBs = $\ln(FSR/Peak-to-Peak\ Noise)/\ln(2)$. FSR is full-scale input or output. RMS Noise corresponds to input or output RMS noise. Peak-to-Peak Noise corresponds to input or output peak-to-peak noise.

(3) Settling time refers to the time from power up, reset, input channel change and gain change to valid stable output data.

Table 2 Key Electrical Characteristics

Analog input

The analog differential input can be directly connected to the differential output of the bridge sensor. Because the signal output by the bridge sensor is small, in order to make full use of the input dynamic range of the A / D converter, the gain of the input preamp is large, which is 128. When the reference voltage VREF is 5V, the full-scale differential input voltage corresponding to this gain is $\pm 20\text{mV}$.

Power supply

The digital power supply (DVDD) voltage should be the same as or less than the power supply voltage of the MCU chip to ensure correct serial data communication with the MCU.

The analog power (AVDD) voltage should not be higher than the digital power (DVDD) voltage. Can use the same digital power supply as the MCU chip, and add appropriate isolation when necessary to reduce the interference of digital circuits on analog circuits.

The A / D conversion reference voltage input (VREF) should be connected to the sensor's power supply. This voltage can be taken directly from the analog power supply (AVDD). It can also be supplied by AVDD divided by the resistor and the sensor to reduce the power consumption of the sensor.

Clock selection

The clock of the HX710 chip is provided by the clock oscillator inside the chip. The typical output data rate is 10Hz or 40Hz.

Temperature measurement (HX710A)

The digital temperature sensor inside the HX710A chip can be directly used to read the temperature in the chip, that is, the temperature in the system. Its effective

The (stable) number of digits is 15 digits. Typical temperature measurement accuracy is 20.4 readings (15 digits) per degree ($^{\circ}\text{C}$).

When using a digital temperature sensor, pay attention to the temperature sensor inside the chip. There is a large difference in zero and gain between the chip and the chip. If used to measure absolute temperature, both zero and gain need to be corrected. If the measured temperature is used for system temperature-related performance compensation, zero and gain need not be corrected, as long as the linearity of the temperature measurement meets the requirements.

(DVDD-AVDD) Voltage Difference Measurement (HX710B)

HX710B can be used to measure (DVDD-AVDD) voltage difference. If DVDD is directly connected to the battery output and AVDD is provided by the regulator output, then the HX710B can be used to directly measure the battery voltage without any external components.

Serial communication

The serial communication line is composed of pins PD_SCK and DOUT, which are used to output data, select the output data rate and input signal.

When the data output pin DOUT is high, it indicates that the A / D converter is not ready to output data.

At this time, the serial clock input signal PD_SCK should be low. After DOUT changes from high to low, PD_SCK should input 25 to 27 different clock pulses (Figure 2). The rising edge of the first clock pulse will read out and output the most significant bit of 24-bit data

(MSB) until the 24th clock pulse is completed, and 24-bit output data is output bit by bit from the highest bit to the lowest bit. The 25th to 27th clock pulses are used to select the output data rate and input signal for the next A / D conversion. See Table 3.

PD_SCK pulse number	Input selection	Speed rate
25	Differential signal	10 Hz
26	Temperature measurement (HX710A)	40 Hz
26	DVDD-AVDD measurement (HX710B)	40 Hz
27	Differential signal	40 Hz

Table 3 Input selection and output data rate selection

The number of input clock pulses of PD_SCK should not be less than 25 or more than 27, otherwise it will cause serial communication errors.

When the input signal or output data rate of the A / D converter changes, the A / D converter needs 4 data output cycles to stabilize. DOUT will change from high level to low level after 4 data output cycles, and output valid data.

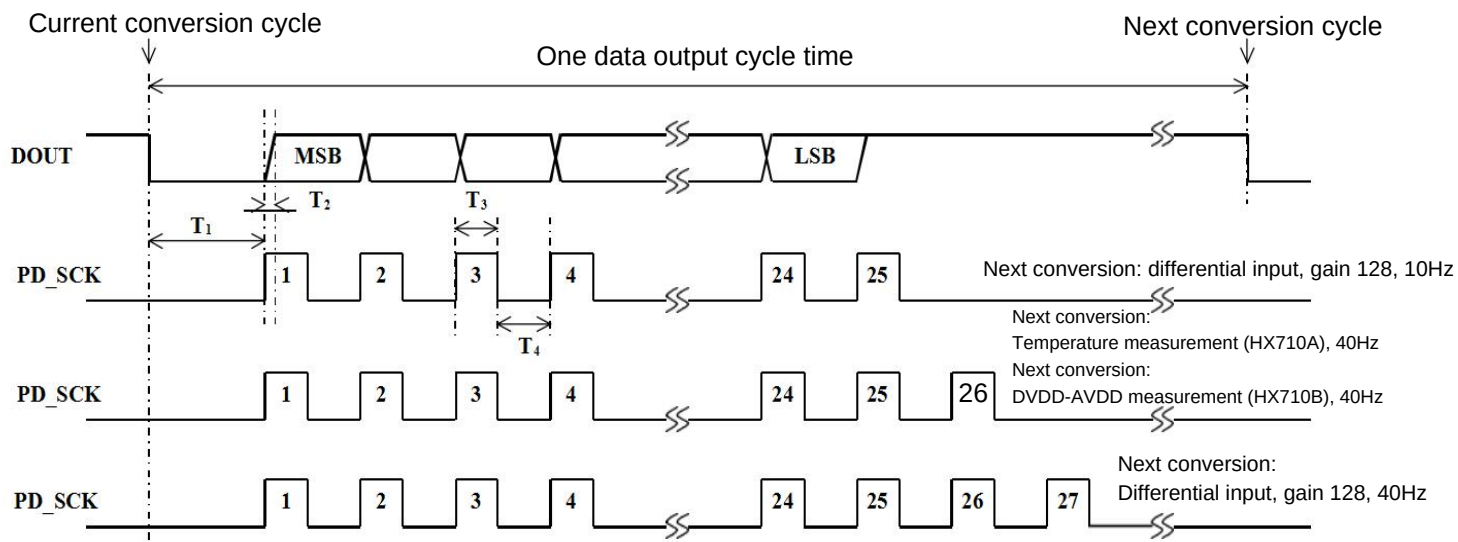


Figure 2 Timing chart of data output, input channel and gain selection

Symbol	Description	Min.	Typ.	Max.	Unit
T ₁	DOUT falling edge to PD_SCK pulse rising edge	0.1			μs
T ₂	PD_SCK pulse rising edge to DOUT data valid			0.1	μs
T ₃	PD_SCK Positive Pulse Level Time	0.2		50	μs
T ₄	PD_SCK Negative Pulse Level Time	0.2			μs

Reset and power down

When the chip is powered on, the power-on automatic reset circuit inside the chip will automatically reset the chip.

The PD_SCK pin is used to control the power off of the HX710. When PD_SCK is low, the chip is in normal working state.

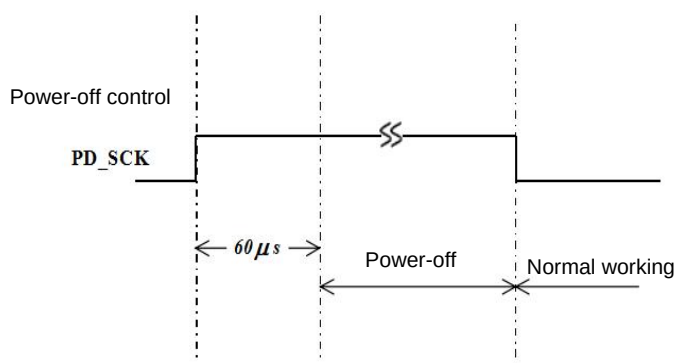


Figure 3: Power-off control

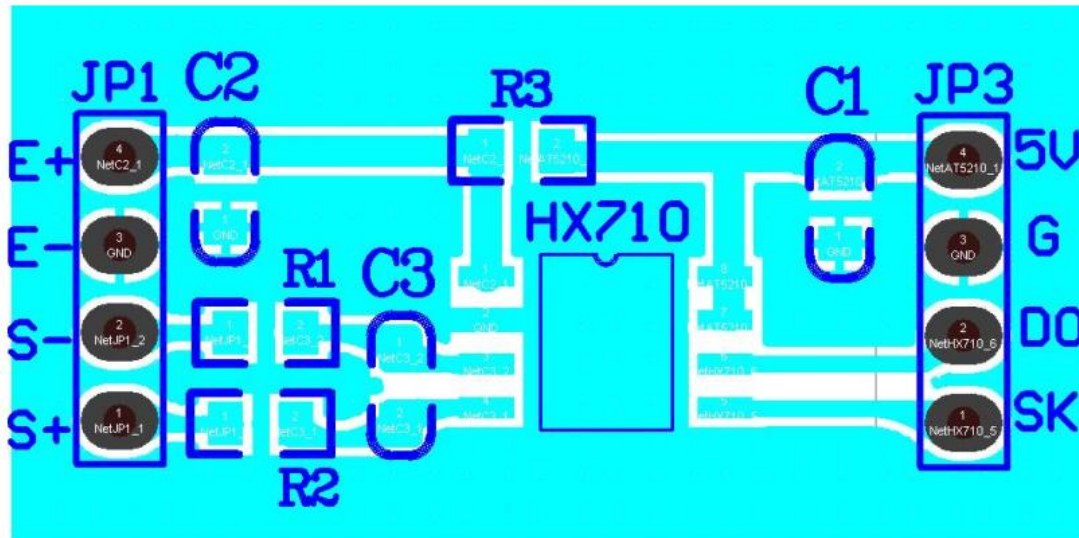
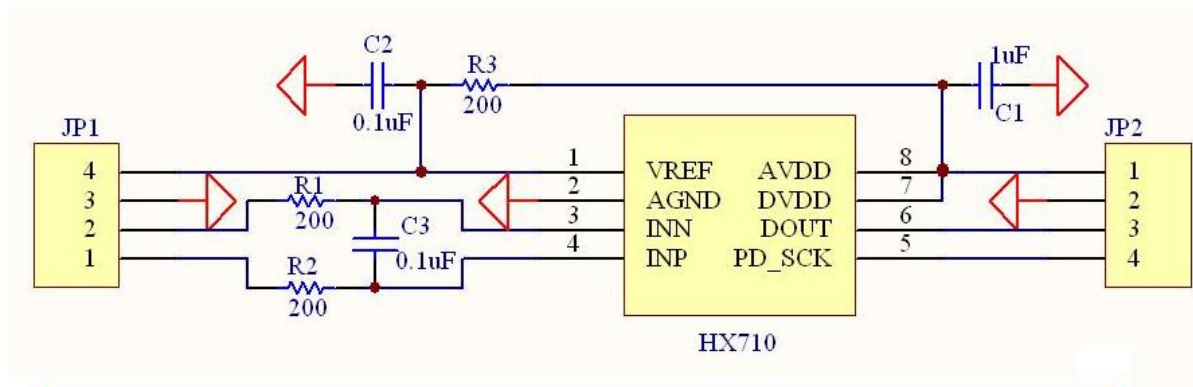
If PD_SCK changes from low level to high level and stays at high level for more than 60μs, HX710 enters power-off state (Figure 3). When PD_SCK returns to low level, the chip will enter the normal working state again. After the chip returns from the power-off state to the normal working state, if the conversion rate and input signal selection before power-off are to be maintained, the power-off cannot be performed in the current data conversion cycle where the number of clock pulses changes. Instead, it should be performed on or after the next data conversion cycle after the number of clock pulses has changed.

After the chip enters the normal working state from the reset or power-off state, the A / D converter needs 4 data output cycles to stabilize. DOUT will change from high level to low level after 4 data output cycles, and output valid data.

Applications

Figure 1 is a typical scheme of HX710 chip applied to electronic scales.

This solution uses a voltage regulator to power the ADC and MCU at the same time, which can be used for LED display and LCD display.



Reference driver: (assembly)

```

/*-----
Called in ASM:      LCALL   ReadAD
Can be called in C:  extern unsigned long ReadAD(void);

                    .
                    .
                    unsigned long data;
                    data=ReadAD();
                    .
                    .
-----*/

PUBLIC      ReadAD
HX710ROM    segment   code
rseg        HX710ROM

```

```

sbit      ADD0 = P1.5;
sbit      ADSK = P0.0;

/*-----
OUT:  R4, R5, R6, R7  R7=>LSB
If called in C, R4, R5, R6, R7 cannot be modifie.
-----*/
ReadAD:
    CLR    ADSK                //Enable AD (PD_SCK goes low)
    SETB   ADD0                //51CPU quasi-bidirectional I / O input enable
    JB     ADD0, $              //Determine if AD conversion is complete, if not, wait or else start reading
    MOV    R4, #24
ShiftOut:
    SETB   ADSK                // Set PD_SCK high (send pulse)
    NOP
    CLR    ADSK                //PD_SCK low
    MOV    C, ADD0              //Read data (one bit at a time)
    XCH    A, R7                //Move in data
    RLC    A
    XCH    A, R7
    XCH    A, R6
    RLC    A
    XCH    A, R6
    XCH    A, R5
    RLC    A
    XCH    A, R5
    DJNZ   R4, ShiftOut        //Judge whether to move into 24BIT
    SETB   ADSK
    NOP
    CLR    ADSK
    RET
    END

```

Reference driver program(C)

```

sbit  ADD0 = P1^5;
sbit  ADSK = P0^0;
unsigned long ReadCount(void) {
    unsigned long Count;
    unsigned char i;
    ADD0=1;          // Non-type 51 MCU, skip this line
    ADSK=0;
    Count=0;
    while(ADD0);
    for (i=0;i<24;i++) {
        ADSK=1;
        Count=Count<<1;
        ADSK=0;
        if(ADD0) Count++;
    }
    ADSK=1;
}

```

```
Count=Count^0x800000;  
ADSK=0;  
return(Count);  
}
```

